Remarks

In view of the above amendments and the following remarks, reconsideration and further examination are requested.

Claims 1 and 2 have been rejected under 35 U.S.C. §102(e) as being anticipated by Cho (US 6,158,039).

Claim 3 has been indicated as containing allowable subject matter. The Applicant would like to thank the Examiner for this indication of allowable subject matter.

Claim 1 has been amended so as to further distinguish the present invention from the reference relied upon in the rejection.

In addition, claims 1-3 have been amended to make a number of editorial revisions. These revisions have been made to place the claims in better U.S. form. None of these amendments have been made to narrow the scope of protection of the claims, nor to address issues related to patentability and therefore, these amendments should not be construed as limiting the scope of equivalents of the claimed features offered by the Doctrine of Equivalents.

The above-mentioned rejection is submitted to be inapplicable to the claims for the following reasons.

Claim 1 is patentable over Cho, since claim 1 recites a signal processor including, in part, a descrambling/error detection unit operable to perform descrambling processing to the data which is stored in a first memory and has been subjected to first error correction, and execute error detection to the data after the descrambling processing; a second memory operable to sequentially store the data which has been subjected to the descrambling processing; an error correction unit operable to perform the first error correction to the data stored in the first memory and perform second error correction to the data in the second memory if necessary; and a controller operable to transmit error-free data which has been stored in the second memory to a host computer, wherein, when the descrambling/error detection unit judges that there is an error in the data which has been subjected to the descrambling processing, the data stored in the second memory are read out for each predetermined error correction block, and subjected to error correction by the error correction unit, and when the descrambling/error detection unit judges that there is no error in the data which has

been subjected to the descrambling processing, the error correction unit does not perform the second error correction, and the controller transmits the data stored in the second memory to the host computer. Cho fails to disclose or suggest an error correction unit and a descrambling/error detection unit as recited in claim 1.

Cho discloses a system decoder 18 having an ECC memory controller 108, a third memory 130, a fourth memory 140, an error corrector 110, a descrambler and error detector 112, a buffer write controller 114, a microprocessor memory access controller 116, a buffer read controller 118, and a second memory 30. The ECC memory controller 108 receives demodulated data from an EMF demodulator 100. The system decoder 18 operates such that the controller 108 writes one correcting block of the received demodulated data into the third memory 130 in a first step. In the next step, the error corrector 110 error-corrects the data written in the third memory 130 and the controller 108 writes the next correcting block of the received demodulated data into the fourth memory 140. In the next step, the error corrector 110 error-corrects the data written in the fourth memory 140, and the controller 108 simultaneously outputs the error-corrected data from the third memory 130 to the descrambler and error detector 112 and inputs the next correcting block of the received demodulated data to the third memory 130. In the next step, the error corrector 110 error-corrects the data written in the third memory 130, and the controller 108 simultaneously outputs the error-corrected data from the fourth memory 140 to the descrambler and error detector 112 and inputs the next correcting block of the demodulated data to the fourth memory 140. This process is repeated until the demodulated data is no longer received from the EMF demodulator 100.

The descrambler and error detector 112 alternatively receives the error-corrected data from the third memory 130 and the fourth memory 140 and restores the data scrambled during an encoding process and detects any errors in the descrambled data. The buffer write controller 114 under control of the microprocessor memory controller 116 then stores the descrambled data and any error information in the second memory 30. Next, the buffer read controller 118, also under control of the microprocessor memory controller 116, reads the data stored in the second memory 30 and transmits the data to an A/V decoder interface and a DVD-ROM interface 126. (See column 2, lines 38-60; column 3, lines 34-43; column 4, line 38 - column 5, line 21; and Figures 2-4).

As discussed above, the third memory 130 and the fourth memory 140 store the correcting blocks both before and after the error corrector 110 makes corrections thereto. However, it is apparent that the third memory 130 and the fourth memory 140 do not store the data of the correcting blocks after the data is descrambled and error detected by the descrambler and error detector 112. This is illustrated in Figure 3 of Cho which clearly has a one-way arrow pointing from the ECC memory controller 108 towards the descrambler and error detector 112. (See Figure 3).

Claim 1 recites that the second memory is operable to sequentially store data which has been subjected to descrambling processing. Therefore, it is apparent that neither the third memory 130, nor the fourth memory 140, can correspond to the claimed second memory because the third memory 130 and the fourth memory 140 both store the correcting blocks before the data contained therein is descrambled by the descrambling and error detector 112. Further, the one-way arrow from the ECC memory controller 108 towards the descrambling and error detector 112 indicates that once the data from the correcting blocks are descrambled by the descrambling and error detector 112, the descrambled data is not then sent back to the third memory 130 or the fourth memory 140. As a result, the only memory of Cho that could potentially correspond to the claimed second memory would be the second memory 30, which is down stream from the descrambling and error detector 112.

The second memory 30 of Cho receives descrambled data and any error information detected by the descrambler and error detector 112 and stores the descrambled data and the error information. The descrambled data in the second memory 30 is read out and transmitted to the A/V decoder interface and the DVD-ROM interface 126. In other words, even though the descrambler and error detector 112 might detect an error in the descrambled data and this error information is stored in the second memory 30, no error correction is performed on the descrambled data. Instead, the descrambled data in the second memory 30 is transmitted to the A/V decoder interface and the DVD-ROM interface 126 regardless of whether or not an error has been detected.

Claim 1 recites an error correction unit operable to perform first error correction to the data stored in a first memory and perform second error correction to the data in a second memory if necessary. Cho does disclose the error corrector 110 that corrects errors in the correcting blocks

stored in the third memory 130 and the fourth memory 140. However, the error corrector 110 does not correct errors in the descrambled data stored in the second memory 30, which, as discussed above, is the only memory of Cho that could potentially correspond to the second memory claimed in claim 1. That the error corrector 110 cannot correct the descrambled data stored in the second memory 30 is clearly illustrated by the one-way arrows from the ECC memory controller 108 to the buffer write controller 114 in Figure 3 of Cho. As a result, the error corrector 110 cannot correspond to the claimed error correction unit because it cannot perform the recited second error correction.

Claim 1 also recites that when a descrambling/error detection unit judges that there is an error in the data which has been subjected to the descrambling processing, the data stored in the second memory are read out for each predetermined error correction block, and subjected to error correction by the error correction unit, and when the descrambling/error detection unit judges that there is no error in the data which has been subjected to the descrambling processing, the error correction unit does not perform the second error correction, and a controller transmits the data stored in the second memory to the host computer. Cho does disclose that the descrambler and error detector 112 detects errors in the descrambled data. However, the descrambler and error detector 112 unconditionally sends the descrambled data and any error information to the second memory 30, where it is stored. The descrambled data in the second memory 30 is then read out and transmitted to the A/V decoder interface and the DVD-ROM interface 126. In other words, even though the descrambler and error detector 112 might detect an error in the descrambled data and this error information is stored in the second memory 30, no error correction is performed on the descrambled data. Instead, the data in the second memory 30 is transmitted to the A/V decoder interface and the DVD-ROM interface 126 regardless of whether or not an error has been detected. Therefore, Cho fails to disclose or suggest these features of claim 1.

As a result, it is apparent that Cho fails to disclose or suggest the present invention as recited in claim 1.

Because of the above-mentioned distinctions, it is believed clear that claims 1-3 are not anticipated by Cho. Furthermore, it is submitted that the distinctions are such that a person having ordinary skill in the art at the time of invention would not have been motivated to modify Cho or to

make any combination of the references of record in such a manner as to result in, or otherwise render obvious, the present invention as recited in claims 1-3. Therefore, it is submitted that claims 1-3 are clearly allowable over the prior art of record.

In view of the above amendments and remarks, it is submitted that the present application is now in condition for allowance. The Examiner is invited to contact the undersigned by telephone if it is felt that there are issues remaining which must be resolved before allowance of the application.

Respectfully submitted,

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